CECS 341

Lab 1

Eugene Paul Mesina



* **Section A:** MUX

//////////////////////////////////

//Student: Eugene Mesina

//Class: 341

//Professor: Xiaolong Wu

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module mux(

input In0,

input In1,

input In2,

input In3,

input [1:0] Sel,

output reg Out

);

always @(In0, In1, In2, In3, Sel)

case (Sel)

0: Out <= In0;

1: Out <= In1;

2: Out <= In2;

3: Out <= In3;

endcase

endmodule

* **Section B:** Mux Tester

`timescale 1ns / 1ps

//////////////////////////////////

//Student: Eugene Mesina

//Class: 341

//Professor: Xiaolong Wu

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module muxvtf;

// Inputs

reg In0;

reg In1;

reg In2;

reg In3;

reg [1:0] Sel;

// Outputs

wire Out;

// Instantiate the Unit Under Test (UUT)

mux uut (

.In0(In0),

.In1(In1),

.In2(In2),

.In3(In3),

.Sel(Sel),

.Out(Out)

);

initial begin

// Initialize Inputs

In0 = 0;

In1 = 0;

In2 = 0;

In3 = 0;

Sel = 0;

// Wait 100 ns for global reset to finish

#100;

// Add stimulus here

#100 Sel = 0; In0 = 1;

#100 Sel = 1; In0 = 0; In1 = 1;

#100 Sel = 2; In0 = 0; In1 = 0; In2 = 1;

#100 Sel = 3; In0 = 0; In1 = 0; In2 = 0; In3 = 1;

//

#100 Sel = 0; In0 = 0; In1 = 1; In2 = 1; In3 = 1;

#100 Sel = 1; In0 = 1; In1 = 0; In2 = 1; In3 = 1;

#100 Sel = 2; In0 = 1; In1 = 1; In2 = 0; In3 = 1;

#100 Sel = 3; In0 = 1; In1 = 1; In2 = 1; In3 = 0;

//zero out

#100 Sel = 0; In0 = 0; In1 =0; In2 = 0; In3 = 0;

end

endmodule

